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By: Sunil Dutt
Sunil A. Dutt

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[ ] continuation patent application of
[ ] divisional patent application of
[ ] continuation-in-part patent application of

Inventor(s)/Applicant Identifier: Sharp et al.

For: HYDROGEN ANNEAL FOR CREATING AN ENHANCED TRENCH FOR TRENCH MOSFETS

Enclosed are:
☒ 9 page(s) of specification
☒ 5 page(s) of claims
☒ 1 page of Abstract
☒ 4 sheet(s) of [ ] formal ☒ informal drawing(s).
☒ An assignment of the invention to Fairchild Semiconductor Corporation
☒ A ☒ signed [ ] unsigned Declaration & Power of Attorney
[ ] A [ ] signed [ ] unsigned Declaration.
[ ] A Power of Attorney by Assignee with Certificate Under 37 CFR Section 3.73(b).
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application.
[ ] Notification of change of [ ] power of attorney [ ] correspondence address filed in prior application.
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INDEP. CLAIMS	5	- 3	= *2	x $39.00 =		OR	x $78.00 =	$156.00
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Respectfully submitted,
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UNITED STATES PATENT APPLICATION

HYDROGEN ANNEAL FOR CREATING AN ENHANCED TRENCH FOR TRENCH MOSFETS

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HYDROGEN ANNEAL FOR CREATING AN ENHANCED TRENCH FOR TRENCH MOSFETS

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor technology, and in particular to forming an enhanced trench for applications such as trench MOSFETs (Metal Oxide Semiconductor Field Effect Transistors).

Power field effect transistors, such as MOSFETs are well known in the semiconductor industry. One type of MOSFET is a trench MOSFET. Trench MOSFETs typically include a substrate upon which an epitaxial layer is grown; doped source regions of a first charge type (i.e. p or n); a doped well of an opposite charge type from the source regions; one or more trenches that extend into the body of the well(s); a dielectric layer covering the inner wall(s) of the trench(es); a conductive material (e.g. polysilicon) covering the inner wall(s) of the dielectric layer(s), which embody the gate(s) of the trench MOSFET(s); and one or more optional doped heavy body (bodies) of the same charge type as the well(s).

It is desirable that a trench, formed in the fabrication of a trench MOSFET, extend substantially vertically into the body of the well(s). This allows a higher density of trenches to be formed across the semiconductor substrate. Because an anisotropic etch etches substantially in one direction, it is preferred compared to other isotropic etches.

One undesirable side effect that results from use of an anisotropic etch, however, is the sharp edges that form along the top and bottom corners of the trench. If the trench has sharp edges at its corners, it becomes difficult to grow a gate oxide that is uniform in thickness. A gate oxide that varies in thickness becomes subject to nonuniform electric fields along the trench MOSFET channel region, which degrades the performance of the trench MOSFET. This is exacerbated by the fact that a trench MOSFET is typically made up of a large number of trenches, either in a stripped or cellular pattern. In a trench MOSFET, wherein all trenches are fabricated without rounded corners, the peak electric fields tend to move towards the trench corners. By

contrast, a series of trenches having rounded corners causes the peak electric fields to move away from the trench corners and toward central locations between adjacent trenches.

One method of smoothing out the corners of a trench is to administer a rounding etch to the trench followed by a downstream plasma etch. However this method, can cause added damage to the silicon and introduces several additional processing steps in the overall process of manufacturing the rounded trench.

It would be desirable, therefore, if a solution were available that could round the trench corners without having to add additional processing steps in the overall process of forming the enhanced trench.

Another critical step in the manufacture of a trench MOSFET is the forming of an oxide layer for the gate electrode, which is as defect-free as possible. This requires that the underlying silicon, upon which the oxide layer is to be grown, itself be as crystalline and as defect-free as possible, so that traps or other defects do not readily form at the silicon/dielectric interface and/or propagate into the dielectric material as it is grown. Such defects can increase the charge density in the oxide layer, thereby lowering the gate oxide breakdown voltage (often characterized by charge breakdown, QBD). A low QBD signifies a trench MOSFET with degraded performance capabilities.

To achieve a high-quality gate oxide with a high QBD, the native oxide that forms on the walls of the silicon trench is typically removed, after which a high-quality gate oxide is grown using thermal oxidation. (A "native oxide" is an oxide that naturally grows on a bare silicon surface when it is exposed to air.) While a native oxide is for the most part crystalline, it is also prone to defect capture and retention.

One method of removing the native oxide is to perform a wet etch using hydrofluoric (HF) acid. However, use of HF is undesirable in that it not only leaves behind impurity byproducts associated with fluorine, it also calls for additional processing steps (e.g. cleaning steps including washing and drying).

Another prior art method of preparing the trench for gate oxidation is to grow a sacrificial oxide, whereby an oxide is grown and then stripped to remove defects.

Unfortunately, just as with the HF etch, such a method requires additional processing steps.

It would be desirable, therefore, if a solution were available that could both prepare the walls of the silicon trench for growing a high-quality gate oxide and, at the same time, round the corners of the trench without having to add additional processing steps in the overall process of manufacturing the trench.

The present invention addresses these problems, by rendering unnecessary the previously required prior art rounding and plasma etch steps (used to round the trench corners) and HF or sacrificial oxide and strip steps (to effect defect reduction prior to growing the gate oxide).

SUMMARY OF THE INVENTION

The present invention provides a method of forming a trench in an epitaxial layer grown on a semiconductor substrate, the trench having rounded corners at the top and bottom ends of the trench. The rounded corners are formed, following formation of the trench by an anneal process, which is preferably performed at a combined high temperature and low pressure so as to prevent the epitaxial layer from melting but is sufficient enough to cause the atoms of the epitaxial layer to migrate and form low stress relief points at the trench corners. The strains at the corners of the trench corners are believed to be stress relief points, which cause the trench corners to conform to an elliptical (or "round") shape.

In a first aspect of the invention, a trench is initially formed that extends a predetermined distance into a semiconductor substrate. Preferably, this trench formation step is performed using an anisotropic etch. Following the trench formation step, the trench is annealed, preferably with hydrogen gas. The anneal step has the benefit of not only reducing the defect density on the walls of the trench but also providing the desirable effect of rounding the top and bottom corners of the trench.

In a second aspect of the invention the rounded trench is formed into an epitaxial layer, previously grown on a semiconductor substrate. The process of annealing the trench is substantially similar to the annealing step described in the first aspect of the invention.

In a third aspect of the invention a method of forming a trench with rounded corners is disclosed, which includes the steps of: (a) providing a semiconductor substrate; (b) forming a masking layer on the major surface of the substrate; (c) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access; (d) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench; (e) removing the selectively etched masking layer; and (f) annealing the trench so that corners at the open and closed ends of the trench become rounded.

In a fourth aspect of the invention, a method of forming a trench MOSFET having trench(es) with rounded corners is disclosed, the rounded corners formed using the anneal step in accordance with the present invention.

In a fifth aspect of the invention, a trench MOSFET is disclosed, the trench(es) of the trench MOSFET having rounded corners formed using the anneal step in accordance with the present invention.

Other features and advantages of the invention will be apparent from the following detailed description and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow diagram illustrating an exemplary process flow for manufacturing a trench with rounded corners in accordance with the present invention;

Figure 2A is a cross-sectional view of a semiconductor substrate;

Figure 2B is a cross-sectional view of the result of growing an epitaxial layer on the substrate of Figure 2A;

Figure 2C is a cross-sectional view of the results of growing a masking layer on the epitaxial layer of Figure 2B;

Figure 2D is a cross-sectional view of the result of patterning and etching through the photo resist and masking layers of Figure 2C to define a trench opening access;

Figure 2E is a cross-sectional view of the result of performing an anisotropic etch into the trench opening access and through the epitaxial layer to define a trench;

Figure 2F is a cross-sectional view of the result of stripping the photo resist layer of Figure 2E;

Figure 2G is a cross-sectional view of the result of removing the masking layer of Figure 2F; and

Figure 2H is a cross-sectional view of the result of performing an anneal in accordance with the present invention.

Figure 3 is a cross-sectional view of a portion of a trench MOSFET;

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Referring to Figure 1, there is shown a flow diagram illustrating an exemplary process flow for manufacturing a trench with rounded corners according to the present invention. The following description of the steps in the process flow is only exemplary and it should be understood that the scope of the invention is not limited to this particular example. In particular, processing conditions such as temperature, pressure, layer thicknesses, etc. could be possibly varied, without departing from the spirit of the invention.

Additionally, the process flow of Figure 1 is described in terms of forming a single trench. However, it should be recognized that in the case of a trench MOSFET (or other trench applications), one of skill in the art would understand that a series of trenches could be all formed simultaneously. The process flow according to the present invention will be described herein in connection with Figures 2A through 2H.

The first step 200 in the process flow (See Figure 1) is to provide a semiconductor substrate 10. (See Figure 2A.) In this description, the substrate 10 is taken to be, for the sake of example, n-type and having a standard thickness of, for example, 500 μm.

Next, in step 204, an epitaxial layer 20 is grown onto the substrate 10, preferably to a thickness of from about 4 to 10 μm, as is shown in Figure 2B. The resistivity of the epitaxial layer 20 is typically from about 0.1 Ω-cm to 3.0 Ω-cm.

In step 208, a masking layer 30 is formed over the epitaxial layer 20 as shown in Figure 2C. Preferably, the masking layer 30 is a material made of silicon dioxide (SiO_2) and is grown to a thickness of around 1000 Å.

In step 212, the masking layer 30 is patterned using standard photolithography and then selectively etched using, for example, a buffered oxide etch (hydroflouric acid (HF) buffered with ammonium fluoride (NH_4F)). A trench opening access 40 into the masking layer 30 is thus formed to a depth that just reaches the surface of the epitaxial layer 20. The trench opening access width, x, (refer to Figure 2D) is determined by the limitations on the photolithography capabilities employed. Using standard ultraviolet lithography, an exemplary width of the trench opening access is x ~ 0.45 μm.

In step 216, an anisotropic etch is performed. An anisotropic etch, as it is meant here, is a dry etch that etches substantially in one direction, as compared to an isotropic etch, which etches in more than one direction. Hence, in accordance with the present invention, the anisotropic etch step 216 is used to etch a substantially vertical trench 50 into the epitaxial layer. Typically, the dry etch is in the form of a plasma, which is an almost neutral mixture of energetic molecules, ions and electrons that have been excited in a radio-frequency electric field. Different gases are used depending on the material to be etched. The principal consideration is that the reaction products must be volatile. For etching silicon the preferred reactants are Cl, HBr, HeO_2, the preferred pressure is 150 mTorr and the duration of the etch is approximately 235 seconds.

In this exemplary embodiment, the depth, y, of the trench 50 (refer to Figure 2E) is preferably about 1.5 μm and the width, x', of the trench 50, is approximately 0.42 μm at approximately 0.25 μm deep into the trench.

In step 220, the patterned photo resist is stripped and the trench is wet-cleaned to remove debris left over from the previous steps. The end result is shown in Figure 2F.

In step 224, the masking layer 30 is removed using, for example, a wet etch process that is known in the art. The end result of this step is shown in Figure 2G.

Finally, in step 228, an anneal is performed. Preferably, the anneal is performed using hydrogen gas at a temperature of approximately 1100°C and a pressure of approximately 100 Torr (or ~1.3 x 10^4 Pa). Use of hydrogen gas reduces the oxygen of the native oxide layer formed on the walls of the trench. The oxygen reduction process has the effect of tying up dangling bonds on the silicon surface defining the walls of the trench such that the dangling bonds become hydrogen terminated. This condition is desirable, since it allows a higher quality gate oxide to be grown later than what would be grown over the native oxide. Indeed, use of the hydrogen anneal step in the manufacture of a trench MOSFET according to the present invention can improve QBD by approximately three orders of magnitude.

The anneal step has the effect of not only reducing the oxygen of the native oxide layer, it also causes the upper and lower corners of the trench 50 to become rounded.

Other temperatures and pressures can be used in the anneal step 228. For example, the process can also cause the altering of the shape of the corners of the trench 50 at temperatures within the range of 960 to 1160°C and pressures within the range of 40 to 240 Torr (or ~ 5.3 x 10^3 to 3.2 x 10^4 Pa).

The benefits gained from the hydrogen anneal step 228 of the present invention are three-fold. First, the anneal step 228 restores the epitaxial layer surface in the trench to a surface that is substantially defect-free and ready for gate oxide growth via thermal oxidation. Second, the annealing step 228 has the effect of rounding the corners of the trench (See Figure 2H). Finally, since the rounding etch and HF etch or sacrificial oxide steps used in conventional trench formation processes are not needed, the entire enhanced trench manufacturing process can be performed with less processing steps.

It is believed that the silicon rounding phenomenon, which takes place during the hydrogen anneal step 228, is caused by the excitation of silicon atoms near the top and bottom corners of the trench. At elevated temperatures, within the range of, for example, 960 to 1160°C and pressures in the range of, for example, 40 to 240 Torr (~5.3 x 10^3 to 3.2 x 10^4 Pa), not only is kinetic energy conveyed to individual atoms but high

stress points are believed to form at the corners of the trench, which intensify the strain imparted to the silicon bonds as they seek out stress relief positions. These stress relief positions are substantially elliptical (or "round") in shape.

The processing of a trench using the hydrogen anneal process according to the present invention, can be viewed as an independent process module, which can be performed at different points within the process flow of a variety of different trench MOSFET processes. For example, this trench anneal module can be used in the manufacture of a trench MOSFET, as described in the next paragraph, by employing the module prior to formation of the well (body) and source regions of the trench MOSFET. Alternatively, because of its modularity, the trench formation process can also be performed in a different trench MOSFET embodiment, e.g. after formation of the last dopant junction (i.e. after formation of the well, source and heavy body regions).

Figure 3 shows a simplified cross-section of a portion of an exemplary trench MOSFET. Referring to Figure 3, trenches 100 extend into a substrate 102, which typically includes an epitaxial layer (not shown). The susbstrate 102 acts as the drain of the trench MOSFET. Each trench 100 is lined with an electrically insulating or dielectric material 104, such as silicon dioxide (SiO_2), which acts as the gate oxide. The trench 100 is then filled with a conductive material 106, such as polysilicon, which provides the electrode for the gate of the trench MOSFET. A well or body region 108 is formed on top of substrate 102, and source regions 110 are formed on both sides of each trench 100 as shown. A region referred to as heavy body 112 extends between source regions 110 between adjacent trenches 100. Dielectric material 114 covers trench openings and its adjacent source regions. A layer of metal 116 blankets the top surface of the silicon. For an n-channel MOSFET, the doping polarities for the various regions would be as follows: n-type substrate 102 (providing the drain terminal of the transistor), p-type body 108, p+ heavy body 112, and n+ source 110. The active region of the field effect transistor is thus formed between source 110 and substrate (or drain) 102 along the sides of each trench (or gate) 100.

An example of a trench MOSFET process describing in greater detail the various steps before and after the trench formation process module can be found in commonly-assigned U.S. Patent Application No. 08/970,221, entitled "Field Effect Transistor and Method of Its Manufacture," which is hereby incorporated by reference.

Incorporation of the trench process module of the present invention, into the manufacturing process of a trench MOSFET, can, therefore, produce a higher performance trench MOSFET, which displays a more uniform electric field distribution around the gate area and reduced gate leakage currents.

Although the invention has been described in terms of a preferred process and structure, it will be obvious to those skilled in the art that many modifications and alterations may be made to the disclosed embodiment without departing from the invention. For example, one of skill in the art would understand that a p-type substrate and/or p-type epitaxial layer could modify the disclosed process. Also, although the process of the present invention has been described as having a step of growing an epitaxial layer 20 on the starting substrate 10, it need not necessarily be performed. Hence, these modifications and alterations are intended to be considered as within the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and a closed end within the body of the substrate, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the substrate; and

(b) annealing the trench to:

(1) reduce the number of defects in the trench created during the step of forming, and

(2) to round corners at the open and closed ends of the trench.

2. The method of claim 1, wherein the step of annealing is performed using hydrogen gas.

3. The method of claim 2, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

4. The method of claim 1, wherein the step of forming the trench, is performed using an anisotropic etch.

5. The method of claim 4, wherein following the annealing step, the width of the trench away from the rounded ends, remains substantially the same as the width prior to the annealing step.

6. A method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and by a closed end within the body of the substrate, the method comprising the steps of:

(a) providing a substrate;

(b) growing a masking layer on the major surface of the substrate;

(c) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access;

(d) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench;

(e) removing the selectively etched masking layer; and

(f) annealing the trench so that corners at the open and closed ends of the trench become rounded.

7. The method of claim 6, wherein the step of annealing is performed using hydrogen gas.

8. The method of claim 7, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

9. A method of forming a trench in an epitaxial layer of a semiconductor substrate, the trench defined by a closed end at a major surface of the epitaxial layer and a closed end within the body of the epitaxial layer, the method comprising the steps of:

(a) forming a trench that extends a predetermined distance into the epitaxial layer; and

(b) annealing the trench so that corners at the open and closed ends of the trench become rounded.

10. The method of claim 9, wherein the step of annealing is performed using hydrogen gas.

11. The method of claim 10, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

12. The method of claim 9, wherein the step of annealing also functions to reduce the number of material defects in and/or on the walls of the trench.

13. The method of claim 9, wherein the step of forming the trench is performed using an anisotropic etch.

14. The method of claim 13, wherein, following the annealing step, the width of the trench, away from the rounded ends, remains substantially the same as the width prior to the annealing step.

15. A trench field effect transistor, comprising:

(a) a semiconductor substrate of a first dopant charge type, the substrate embodying the drain of the trench field effect transistor;

(b) a body layer of a second dopant charge type, overlaying a major surface of the substrate;

(c) at least one trench having walls extending through the body layer and into the substrate to a first predetermined depth, the at least one trench having a first end at a major surface of the body layer and a second end at the first predetermined depth;

(d) a dielectric having outer walls adjacent the walls of the at least one trench and inner walls;

(e) a conductor covering the inner walls of the dielectric, the conductor embodying the gate of the trench field effect transistor; and

(f) a pair of source regions of the first dopant charge type, extending from the major surface of the body layer to a second predetermined depth within the body layer and positioned adjacent the outer walls of the dielectric,

wherein corners at both the first and second ends of the at least one trench are rounded as the result of an annealing step applied during the process of fabricating the trench field effect transistor.

16. The trench field effect transistor of claim 15, wherein the anneal step applied during the process of fabricating the trench field effect transistor, is performed using hydrogen gas.

17. The trench field effect transistor of claim 16, wherein the anneal step applied during the process of fabricating the trench field effect transistor, is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

18. The trench field effect transistor of claim 15, wherein during the process of fabricating the trench field effect transistor, the at least one trench is formed using an anisotropic etch.

19. A method of making a trench field effect transistor, comprising:

(a) providing a semiconductor substrate of a first dopant charge type, the substrate embodying the drain of the trench field effect transistor;

(b) growing an epitaxial layer of the same first dopant charge type on the substrate, the epitaxial layer having a different resistivity than the resistivity of the substrate;

(c) forming at least one trench into the epitaxial layer, each trench defined by a first end in a plane defined by a major surface of the substrate and by walls that extend to a second end at a predetermined depth into the epitaxial layer;

(d) annealing the at least one trench to:

(1) reduce the number of defects in the at least one trench created during the step of forming the at least one trench, and

(2) round corners at the first and second ends of the at least one trench;

(e) growing a dielectric layer on the walls of the at least one trench;

(f) forming a conductor over the dielectric layer, the conductor embodying the gate of the trench field effect transistor;

(g) patterning the epitaxial layer and implanting a dopant of a second charge type to form wells interposed between adjacent trenches; and

(h) patterning the epitaxial layer and implanting a dopant of the first charge type to form regions that embody the source regions of the field effect transistor.

20. The method of claim 19, further including the step of forming one or more heavy bodies of the second charge type positioned above the wells and between

the source regions, each heavy body forming an abrupt junction with its corresponding well.

21. The method of claim 19, wherein the step of annealing is performed using hydrogen gas.

22. The method of claim 21, wherein the step of annealing is performed within a temperature range of about 960 to 1160°C and within a pressure range of about 40 to 240 Torr.

23. The method of claim 19, wherein the step of forming the at least one trench is performed using an anisotropic etch.

HYDROGEN ANNEAL FOR CREATING AN ENHANCED TRENCH FOR TRENCH MOSFETS

ABSTRACT OF THE DISCLOSURE

A method of forming a trench in a substrate or in an epitaxial layer, previously grown over the semiconductor substrate, wherein an anneal step, using hydrogen gas results in rounded corners without the need for a rounding etch or any other processing steps to round the corners.

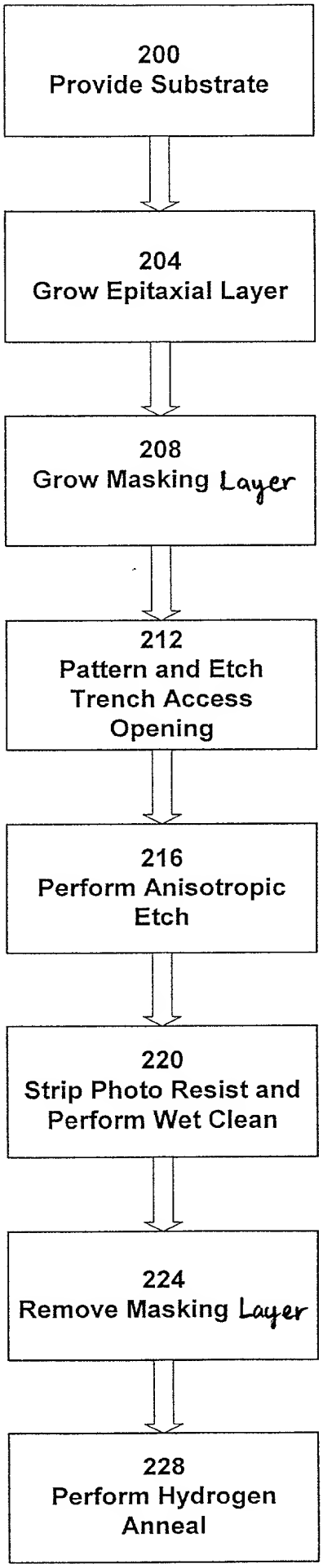

200
Provide Substrate
204
Grow Epitaxial Layer
208
Grow Masking Layer
212
Pattern and Etch
Trench Access
Opening
216
Perform Anisotropic
Etch
220
Strip Photo Resist and
Perform Wet Clean
224
Remove Masking Layer
228
Perform Hydrogen
Anneal

Figure 1

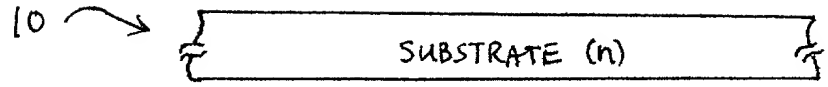


Figure 2A

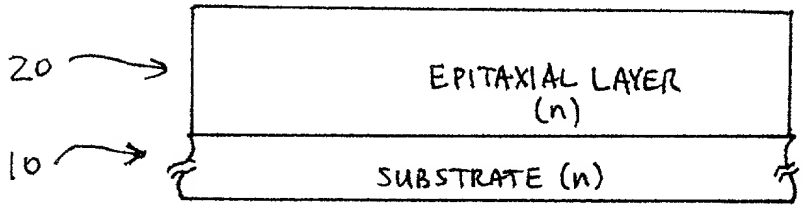
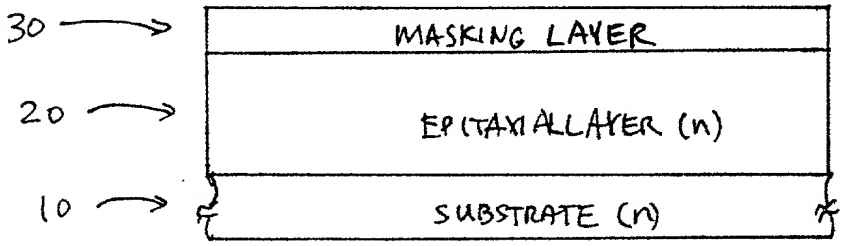


Figure 2B



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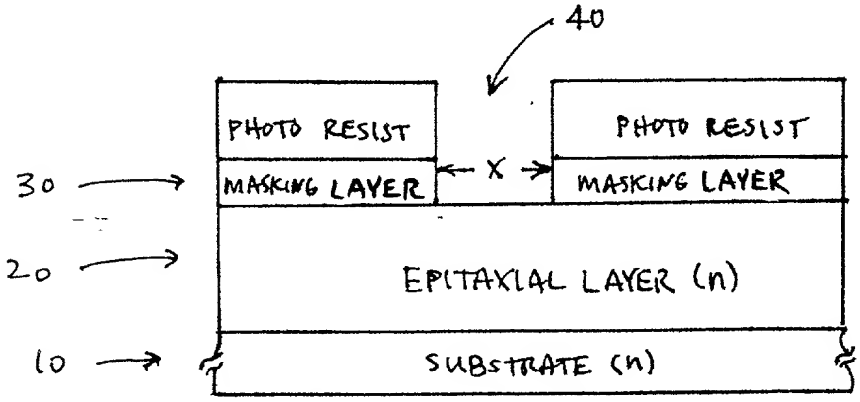

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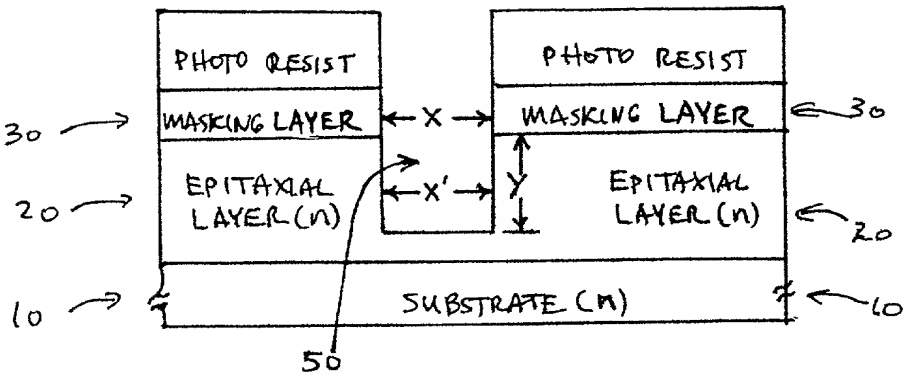

Figure 2E

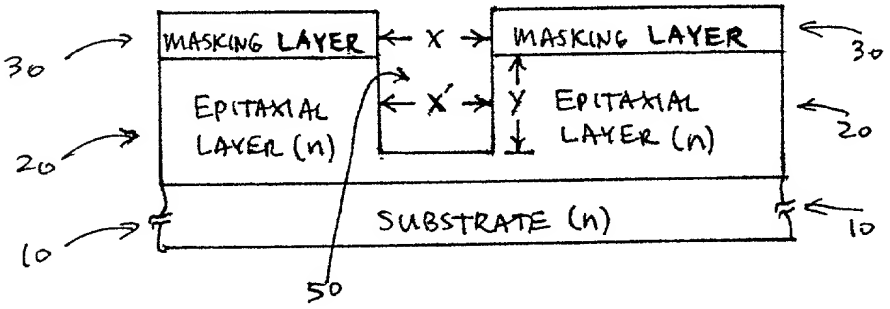

Figure 2F

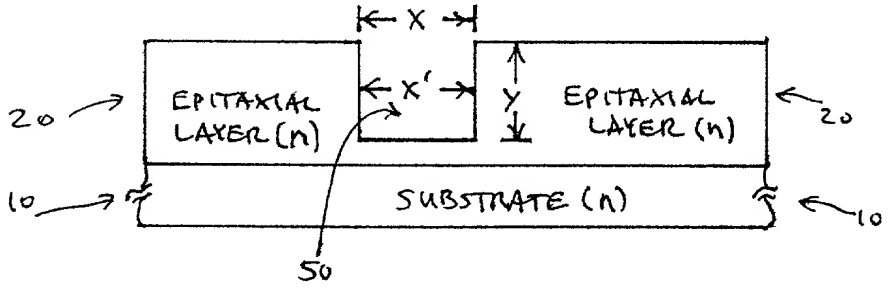

Figure 2G

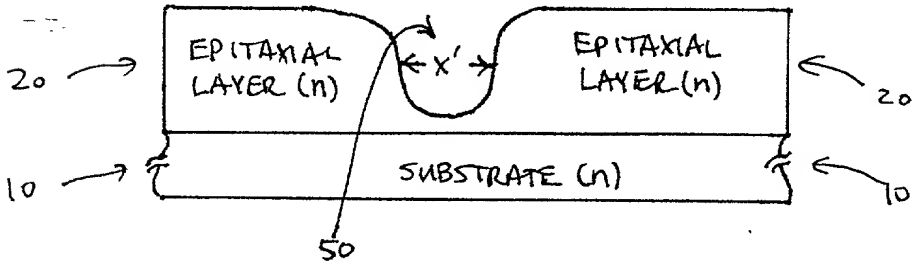

Figure 2H

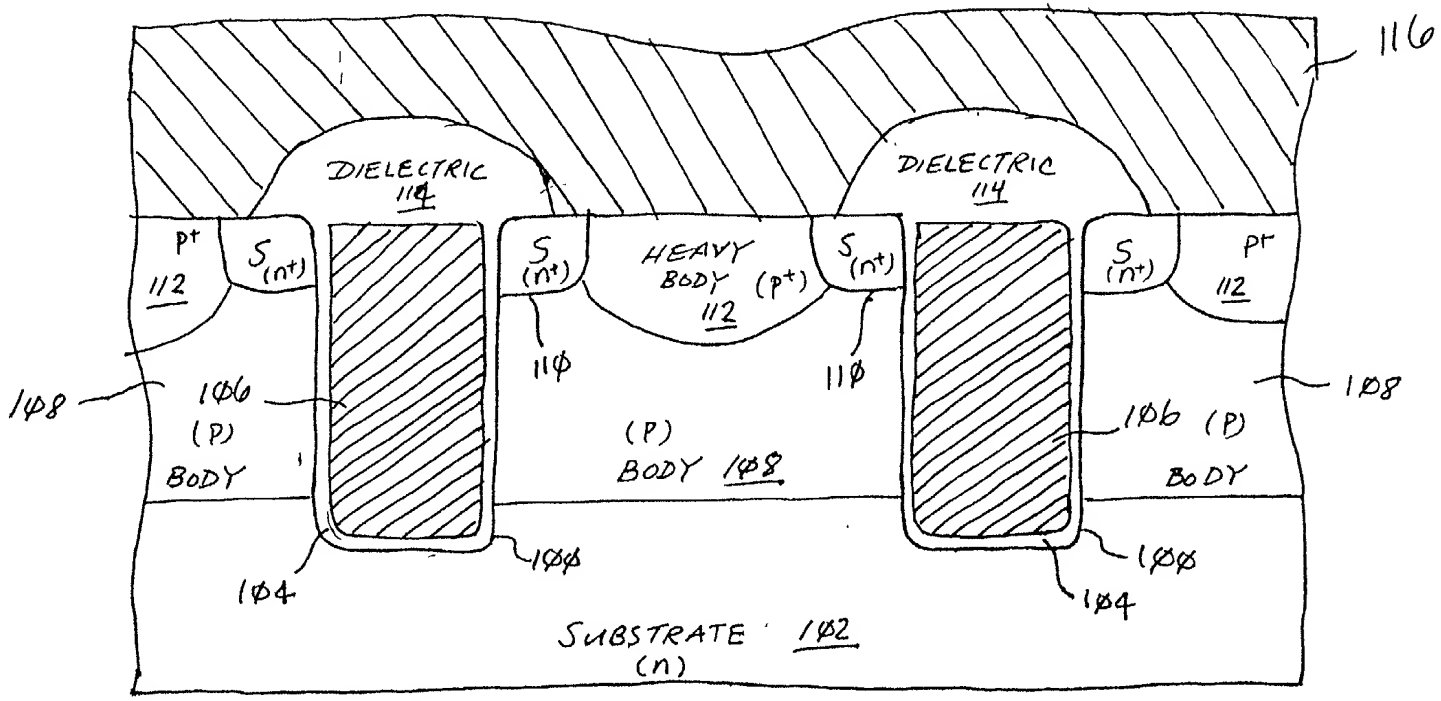

Figure 3

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **HYDROGEN ANNEAL FOR CREATING AN ENHANCED TRENCH FOR TRENCH MOSFETS** the specification of which __XX__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

William E. Winters, Reg. No. 42,232
Babak S. Sani, Reg. No. 37,495

Send Correspondence to:	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2
Joelle Sharp	Gordon K. Madson
JOELLE SHARP	GORDON K. MADSON
Date 10/18/99	Date 10/18/99

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